THE CLAIMS

What is claimed is:

1. A phase detector and signal locking system controller comprising:

a first phase detector receiving at least a first input source and a second input source and outputting at least a first control signal;

a second phase detector receiving at least the first input source and the second input source and outputting at least a second control signal; and

a control unit receiving at least the first control signal, the second control signal, a first gain factor, and a second gain factor and outputting at least a phase measurement result signal.

2. The phase detector and signal locking system controller of claim 1 wherein:

a first operational mode includes the first control signal enabling the application of the first gain factor to the phase measurement result signal; and

a second operational mode includes the second control signal enabling the application of the second gain factor to the phase measurement result signal.

3. A phase detector and signal locking system controller comprising:

a first phase detector receiving at least a first input source and a second input source and outputting at least a first phase indicator signal and a second phase indicator signal;

a second phase detector receiving at least the first input source and the second input source and outputting at least an order indicator signal;

a synchronizing circuit receiving at least the first phase indicator signal, the second phase indicator signal, and a system clock signal and outputting at least a first synchronized phase indicator signal and a second synchronized phase indicator signal; and

a post processing and control unit receiving at least the first synchronized phase indicator signal, the second synchronized phase indicator signal, the order indicator signal and the first input source and outputting a phase measurement result signal.

4. The phase detector and signal locking system controller of claim 3 wherein:

the first phase detector includes a first register, a second register, and a NAND-gate circuit.

5. The phase detector and signal locking system controller of claim 4 wherein:

the first register receives at least the first input source and a reset control signal and outputs at least the first phase indicator signal;

the second register receives at least the second input source and the reset control signal and outputs at least the second phase indicator signal; and

the NAND-gate circuit receives at least the first phase indicator signal and the second phase indicator signal and outputs at least the reset control signal.

6. The phase detector and signal locking system controller of claim 5 wherein:

the first register includes a D-type flip-flop (DFF) circuit having a clk-input, a reset-input, and a Q-output;

the first input source is coupled to at least the clk-input of the DFF circuit;

the reset control signal is coupled to at least the reset-input of the DFF circuit; and

the first phase indicator signal is coupled to at least the Q-output of the DFF circuit.

7. The phase detector and signal locking system controller of claim 5 wherein:

the second register includes a D-type flip-flop (DFF) circuit having a clk-input, a reset-input, and a Q-output;

the second input source is coupled to at least the clk-input of the DFF circuit;

the reset control signal is coupled to at least the reset-input of the DFF circuit; and

the second phase indicator signal is coupled to at least the Q-output of the DFF circuit.

8. The phase detector and signal locking system controller of claim 3 wherein:

the second phase detector includes a register.

9. The phase detector and signal locking system controller of claim 8 wherein:

the register includes a D-type flip-flop (DFF) circuit having a clk-input, a D-input, and a Q-output;

the first input source is coupled to at least the clk-input of the DFF circuit;

the second input source is coupled to at least the D-input of the DFF circuit; and

the order indicator signal is coupled to at least the Q-output of the DFF circuit.

10. The phase detector and signal locking system controller of claim 3 wherein:

the synchronizing circuit includes a first register and a second register.

11. The phase detector and signal locking system controller of claim 10 wherein:

the first register includes a D-type flip-flop (DFF) circuit having a D-input, a clk-input and a Q-output;

the first phase indicator signal is coupled to at least the D-input of the DFF circuit;

the system clock signal is coupled to at least the clk-input of the DFF circuit; and

the first synchronized phase indicator signal is coupled to at least the Q-output of the DFF circuit.

12. The phase detector and signal locking system controller of claim 10 wherein:

the second register includes a D-type flip-flop (DFF) circuit having a D-input, a clk-input, and a Q-output;

the second phase indicator signal is coupled to at least the D-input of the DFF circuit;

the system clock signal is coupled to at least the clk-input of the DFF circuit; and

the second synchronized phase indicator signal is coupled to at least the Q-output of the DFF circuit.

13. The phase detector and signal locking system controller of claim 3 wherein:

the first phase indicator signal is activated upon detection of a first transition edge of the first input source.

14. The phase detector and signal locking system controller of claim 3 wherein:

the second phase indicator signal is activated upon detection of a first transition edge of the second input source.

15. The phase detector and signal locking system controller of claim 3 wherein:

the order indicator signal is activated upon detection of a first transition edge of the second input source occurring prior to the first transition edge of the first input source.

16. The phase detector and signal locking system controller of claim 3 wherein:

the order indicator signal is activated upon detection of the beginning of the period of the second input source occurring prior to the beginning of the period of the first input source.

17. The phase detector and signal locking system controller of claim 3 wherein:

the first synchronized phase indicator signal is activated upon detection of:

a first transition edge of the system clock signal; and

the first phase indicator signal in an active state.

18. The phase detector and signal locking system controller of claim 3 wherein:

the second synchronized phase indicator signal is activated upon detection of:

a first transition edge of the system clock signal; and

the second phase indicator signal in an active state.

19. The phase detector and signal locking system controller of claim 3 wherein the post processing and control unit includes:

a synchronous signal latch receiving at least the first synchronized phase indicator, the second synchronized phase indicator signal, and an edge detection control signal and outputting a first multiplexer selection control signal;

a first multiplexer receiving at least the second synchronized phase indicator signal, the order indicator signal, and the first multiplexer selection control signal and outputting a first multiplexer output signal;

an edge detection block receiving at least the first input source and outputting at least the edge detection control signal;

a first register receiving at least the first multiplexer selection control signal and the edge detection control signal and outputting at least the second multiplexer selection control signal;

a second register receiving at least the first multiplexer output signal and the edge detection control signal and outputting at least a phase result indicator signal;

a programmable storage unit outputting at least a gain combiner value;

a second multiplexer receiving at least the gain combiner value, the second multiplexer selection control signal, and a default gain value and outputting at least a second multiplexer output signal; and

a divider receiving at least the second multiplexer output signal and the phase result indicator signal and outputting at least the phase measurement result signal.

20. The phase detector and signal locking system controller of claim 19 wherein:

the edge detection control signal is activated upon detection of the second transition edge of the first input source.

21. The phase detector and signal locking system controller of claim 19 wherein:

the first multiplexer selection control signal is activated upon detection of:

the first transition edge of the first synchronized phase indicator signal while the second synchronized phase indicator signal is in an inactive state; or

the first transition edge of the second synchronized phase indicator signal while the first synchronized phase indicator signal is in the inactive state.

22. The phase detector and signal locking system controller of claim 19 wherein:

the first multiplexer selection control signal is deactivated upon detection of the edge detection control signal in an active state.

23. The phase detector and signal locking system controller of claim 19 wherein:

the first multiplexer includes a mux circuit having a first input, a second input, a selection input, and an output, and operating to provide the first input to the output when the selection input is in an inactive state and operating to provide the second input to the output when the selection input is in an active state;

the second synchronized phase indicator signal is coupled to at least the second input of the mux circuit;

the order indicator signal is coupled to at least the first input of the mux circuit;

the first multiplexer selection control signal is coupled to at least the selection input of the mux circuit; and

the first multiplexer output signal is coupled to at least the output of the mux circuit.

24. The phase detector and signal locking system controller of claim 19 wherein:

the first register includes a D-type flip-flop (DFF) circuit having a D-input, a clk-input, and a Q-output;

the first multiplexer selection control signal is coupled to at least the D-input of the DFF circuit;

the edge detection control signal is coupled to at least the clk-input of the DFF circuit; and

the second multiplexer selection control signal is coupled to at least the Q-output of the DFF circuit.

25. The phase detector and signal locking system controller of claim 19 wherein:

the second register includes a D-type flip-flop (DFF) circuit having a D-input, a clk-input, and a Q-output;

the first multiplexer output signal is coupled to at least the D-input of the DFF circuit;

the edge detection control signal is coupled to at least the clk-input of the DFF circuit; and

the second multiplexer selection control signal is coupled to at least the Q-output of the DFF circuit.

26. The phase detector and signal locking system controller of claim 19 wherein:

the second multiplexer selection control signal is activated upon detection of:

a first transition edge of the edge detection control signal; and

the first multiplexer selection control signal in an active state.

27. The phase detector and signal locking system controller of claim 19 wherein:

the phase result indicator signal is activated upon detection of:

a first transition edge of the edge detection control signal; and

the first multiplexer output signal in an active state.

28. The phase detector and signal locking system controller of claim 19 wherein:

the second multiplexer includes a mux circuit having a first input, a second input, a selection input, and an output, and operating to provide the first input to the output when the selection input is in an inactive state and operating to provide the second input to the output when the selection input is in an active state;

the default gain value is coupled to at least the first input of the mux circuit;

the gain combiner value is coupled to at least the second input of the mux circuit;

the second multiplexer selection signal is coupled to at least the selection input of the mux circuit; and

the second multiplexer output signal is coupled to at least the output of the mux circuit.

29. The phase detector and signal locking system controller of claim 19 wherein:

the divider includes a divider function circuit having an A-input, a B-input, and a C-output, and operating to provide to the C-output a positive fixed number value divided by the A-input value when the B-input is in an active state and operating to provide to the C-output a negative fixed number value divided by the A-input value when the B-input is in an inactive state;

the second multiplexer output signal is coupled to at least the A-input of the divider function circuit;

the phase result indicator signal is coupled to at least the B-input of the divider function circuit; and

the phase measurement result signal is coupled to at least the C-output of the divider function circuit.

30. The phase detector and signal locking system controller of claim 29 wherein:

the positive fixed number value and the negative fixed number value have the same absolute value.

31. The phase detector and signal locking system controller of claims 13, 14, 15, 17, 18, 21, 26, or 27 wherein:

the first transition edge is the low-to-high signal transition.

32. The phase detector and signal locking system controller of claim 20 wherein:

the second transition edge is the high-to-low signal transition.

33. The phase detector and signal locking system controller of claims 17, 18, 22, 23, 26, 27, 28, or 29 wherein:

the active state is the logic high state.

34. The phase detector and signal locking system controller of claims 21, 23, 28, or 29 wherein:

the inactive state is the logic low state.

35. A means for controlling a signal locking system comprising:

a means for generating a phase measurement result signal by:

applying a first gain factor during a first operational mode controlled by a first phase detector; and

applying a second gain factor during a second operational mode controlled by a second phase detector.

36. A means for controlling a signal locking system comprising:

a means for generating a first phase indicator signal from a first transition edge of a first input source;

a means for generating a second phase indicator signal from the first transition edge of a second input source;

a means for generating a first synchronized phase indicator signal from the first transition edge of a system clock signal and based on the first phase indicator signal in an active state;

a means for generating a second synchronized phase indicator signal from the first transition edge of the system clock signal and based on the second phase indicator signal in an active state;

a means for generating an order indicator signal; and

a means for generating a phase measurement result signal.

37. The means for controlling a signal locking system of claim 36 wherein:

the means for generating the order indicator signal includes means for detecting the first transition edge of the second input source relative to the first transition edge of the first input source.

38. The means for controlling a signal locking system of claim 36 wherein:

the means for generating the phase measurement result signal includes:

means for generating an edge detection control signal based on the second transition edge of the first input source;

means for generating a mode selection result;

means for selecting between the order indicator signal and the second synchronized phase indictor signal based on the mode selection result;

means for generating a gain combiner value and a default gain value;

means for generating a value selection result by selecting between the gain combiner value and the default gain value and based on the mode selection result;

means for generating a phase result indicator signal based on the mode selection result; and

means for applying a divider function to the value selection result based on the phase result indicator signal.

39. The means for controlling a signal locking system of claim 38 wherein:

the means for generating the mode selection result includes:

detection of the first synchronized phase indicator signal in an active state while the second synchronized phase indicator signal is in an inactive state or detection of the second synchronized phase indicator signal in an active state while the first synchronized phase indicator signal is in an inactive state; and

resetting upon detection of the edge detection control signal in an active state.

40. The means for controlling a signal locking system of claims 36 or 37 wherein:

the first transition edge is the low-to-high signal transition.

41. The means for controlling a signal locking system of claim 38 wherein:

the second transition edge is the high-to-low signal transition.

42. The means for controlling a signal locking system of claims 36 or 39 wherein:

the active state is the logic high state.

43. The means for controlling a signal locking system of claim 39 wherein:

the inactive state is the logic low state.

44. A method of controlling a signal locking system comprising the steps of:

generating a phase measurement result signal by:

applying a first gain factor during a first operational mode controlled by a first phase detector; and

applying a second gain factor during a second operational mode controlled by a second phase detector.

45. A method of controlling a signal locking system comprising the steps of:

generating a first phase indicator signal from a first transition edge of a first input source;

generating a second phase indicator signal from the first transition edge of a second input source;

generating a first synchronized phase indicator signal from the first transition edge of a system clock signal and based on the first phase indicator signal in an active state;

generating a second synchronized phase indicator signal from the first transition edge of the system clock signal and based on the second phase indicator signal in an active state;

generating an order indicator signal; and

generating a phase measurement result signal.

46. The method of controlling a signal locking system of claim 45, further comprising the step of:

generating the order indicator signal by detecting the first transition edge of the second input source relative to the first transition edge of the first input source.

47. The method of controlling a signal locking system of claim 45 wherein the step of generating the phase measurement result signal further comprises the steps of:

generating an edge detection control signal based on the second transition edge of the first input source;

generating a mode selection result;

selecting between the order indicator signal and the second synchronized phase indictor signal based on the mode selection result;

generating a gain combiner value and a default gain value;

generating a value selection result by selecting between the gain combiner value and the default gain value and based on the mode selection result;

generating a phase result indicator signal based on the mode selection result; and

applying a divider function to the value selection result based on the phase result indicator signal.

48. The method of controlling a signal locking system of claim 47 wherein the step of generating the mode selection result further comprises the steps of:

detecting the first synchronized phase indicator signal in an active state while the second synchronized phase indicator signal is in an inactive state or detecting the second synchronized phase indicator signal in an active state while the first synchronized phase indicator signal is in an inactive state; and

resetting upon detection of the edge detection control signal in an active state.

49. The method of controlling a signal locking system of claims 45 or 46 wherein:

the first transition edge is the low-to-high signal transition.

50. The method of controlling a signal locking system of claim 47 wherein:

the second transition edge is the high-to-low signal transition.

51. The method of controlling a signal locking system of claims 45 or 48 wherein:

the active state is the logic high state.

52. The method of controlling a signal locking system of claim 48 wherein:

the inactive state is the logic low state.